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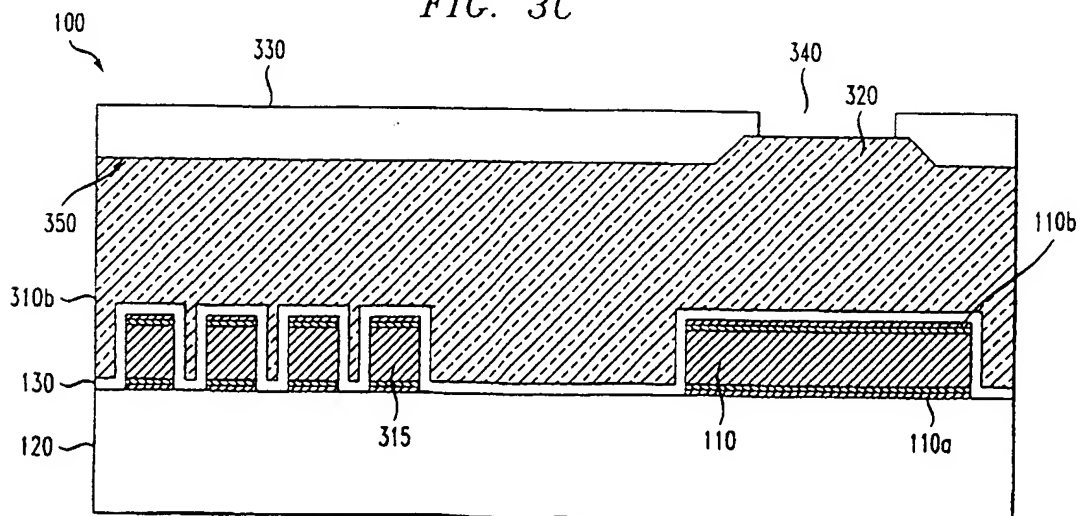INT CL^7 H01L 21/768 23/522 23/532
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(54) Abstract Title
Silicon rich oxides and fluorinated silicon oxide insulating layers

(57) Silicon rich oxide barrier layers are used to encapsulate metal interconnects in an integrated circuit. The barrier layers prevent fluorine diffusing out of a low-k fluorinated silicon glass (FSG) interlayer dielectric which would otherwise react with and damage the metal interconnects. The dielectric layers are deposited using a high density plasma CVD method which can cause the formation of raised bumps 320 over buried features 110. Features greater than about 5000nm in width are difficult to flatten using chemical mechanical polishing, so a photolithographic etching step is used to remove most of such raised features. Subsequently, the ILD may be planarized by CMP.
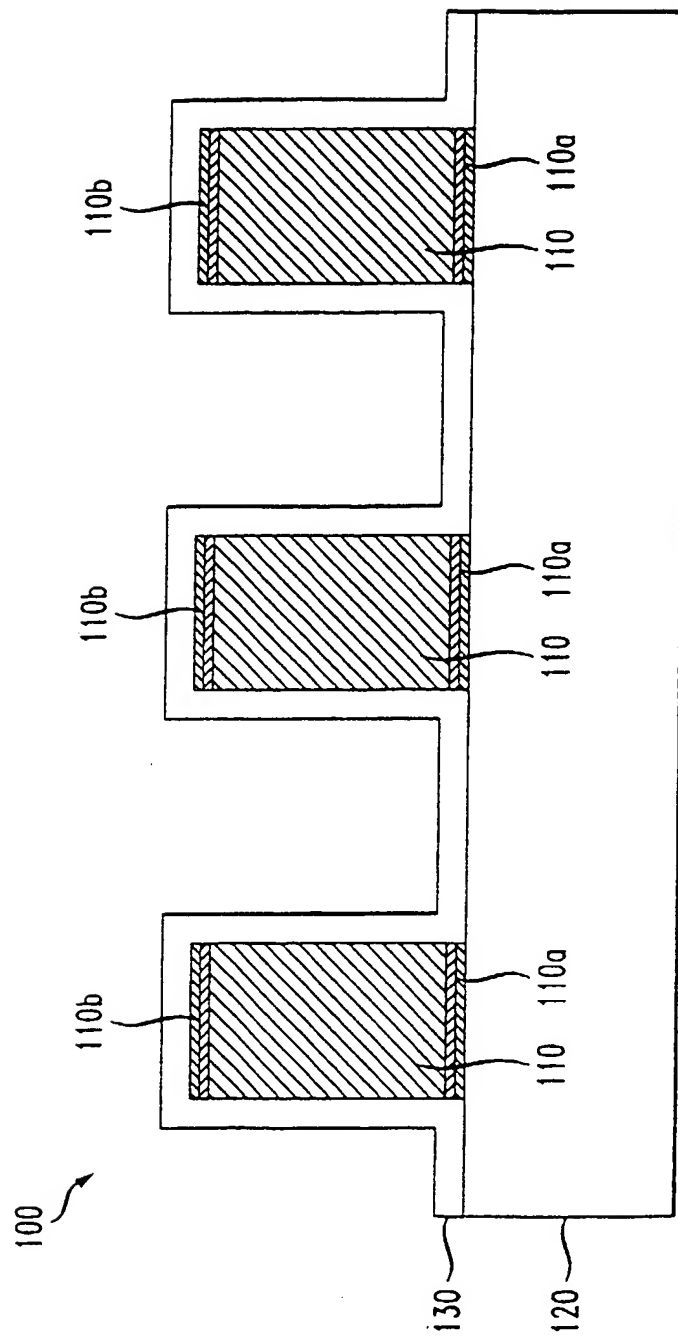
FIG. 3C

GB 2 367 426 A

FIG. 1

FIG. 2

FIG. 3A

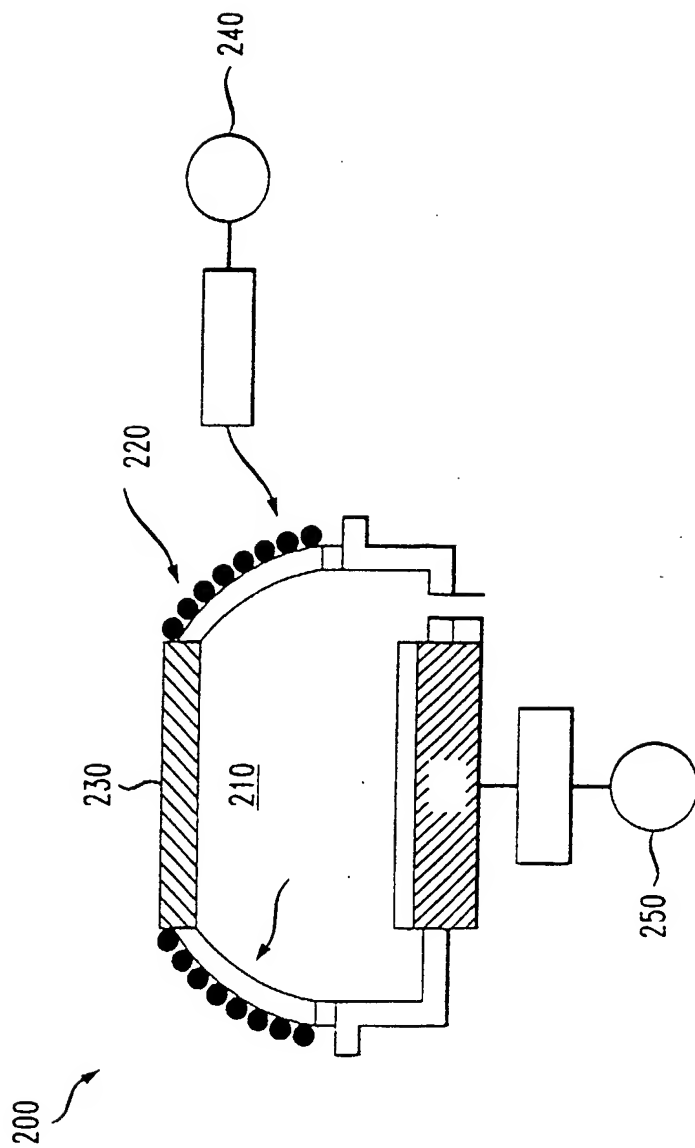*FIG. 3B*

FIG. 3C

110b

340

320

110a

110

330

315

350

310b

130

120

100

FIG. 3D

100

350
310b
130
120

360
360

110b
110a
110
315

FIG. 4

FIG. 5

500

510

560

550

540

530

510a

520b

520b

520b

520

520a

520

520a

520

520a

FIG. 6

600

510
560
550

620
620
540
520
610
635
633

625
623
630
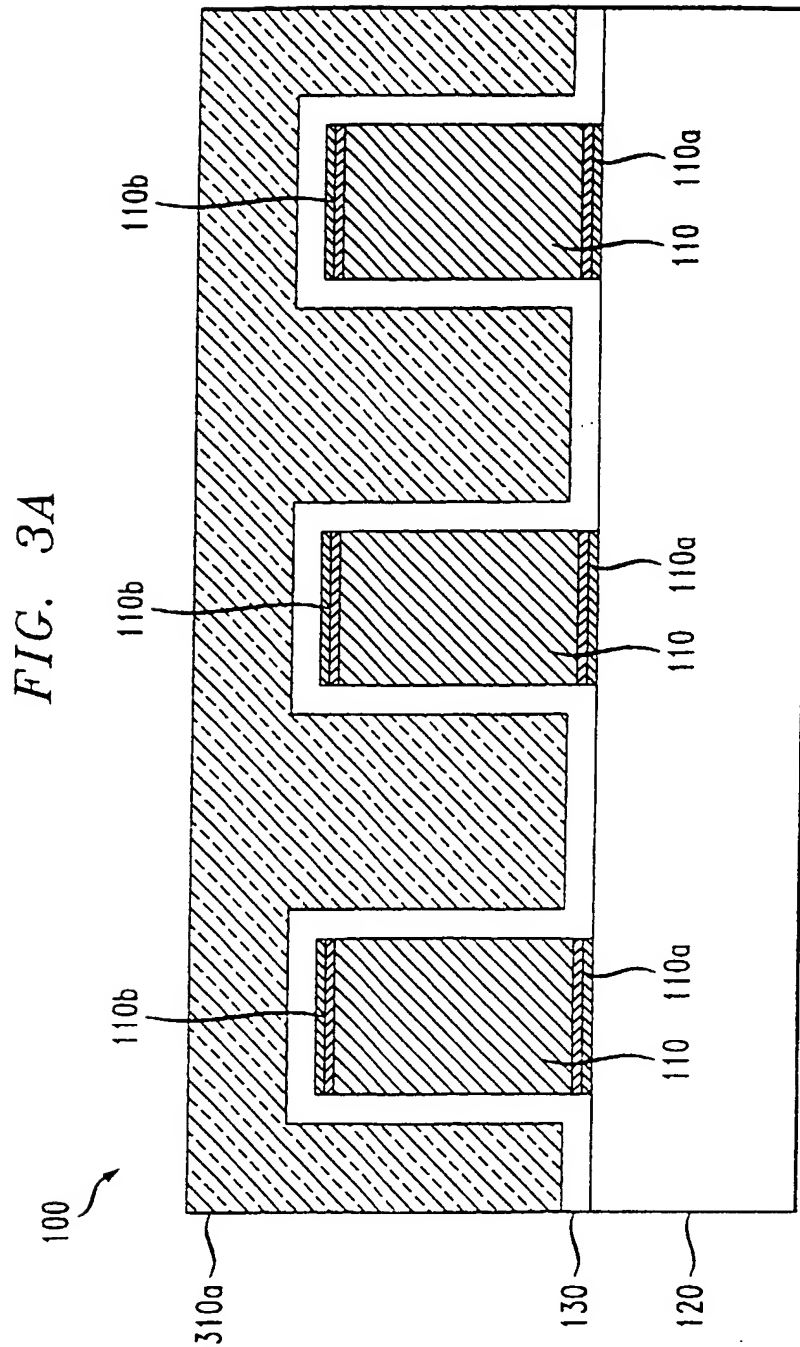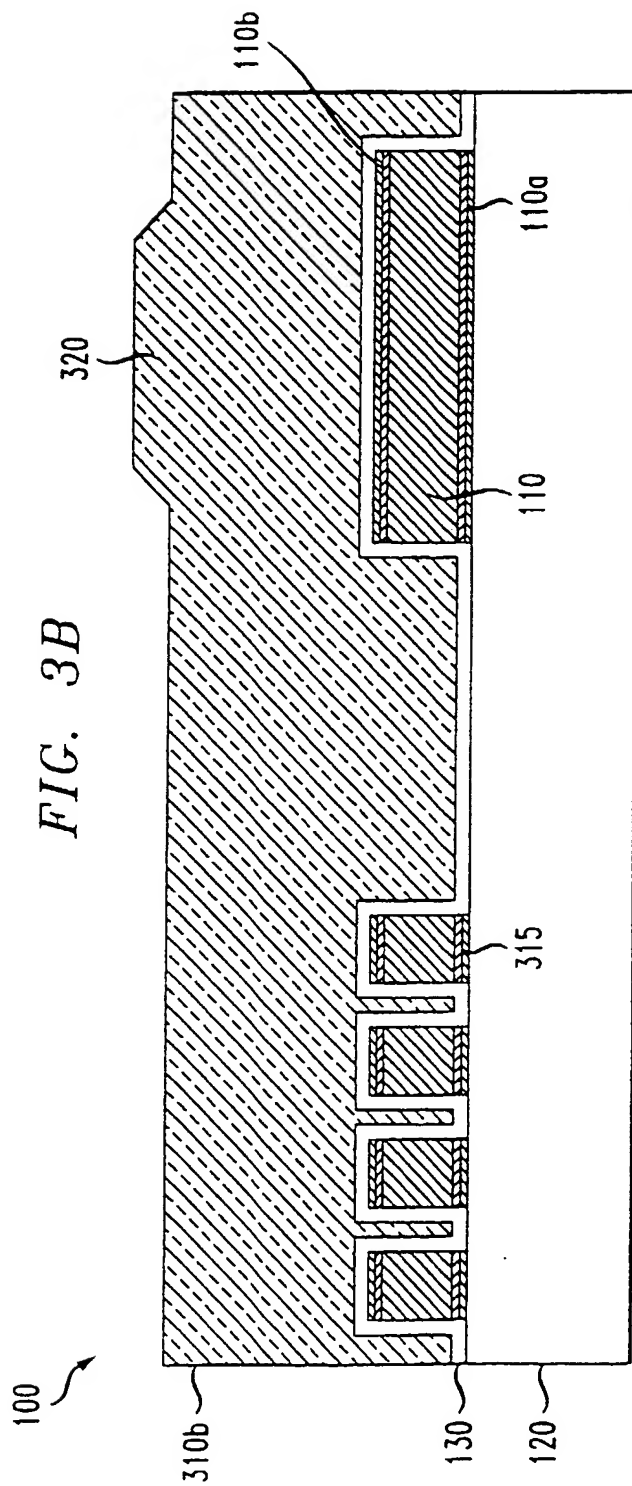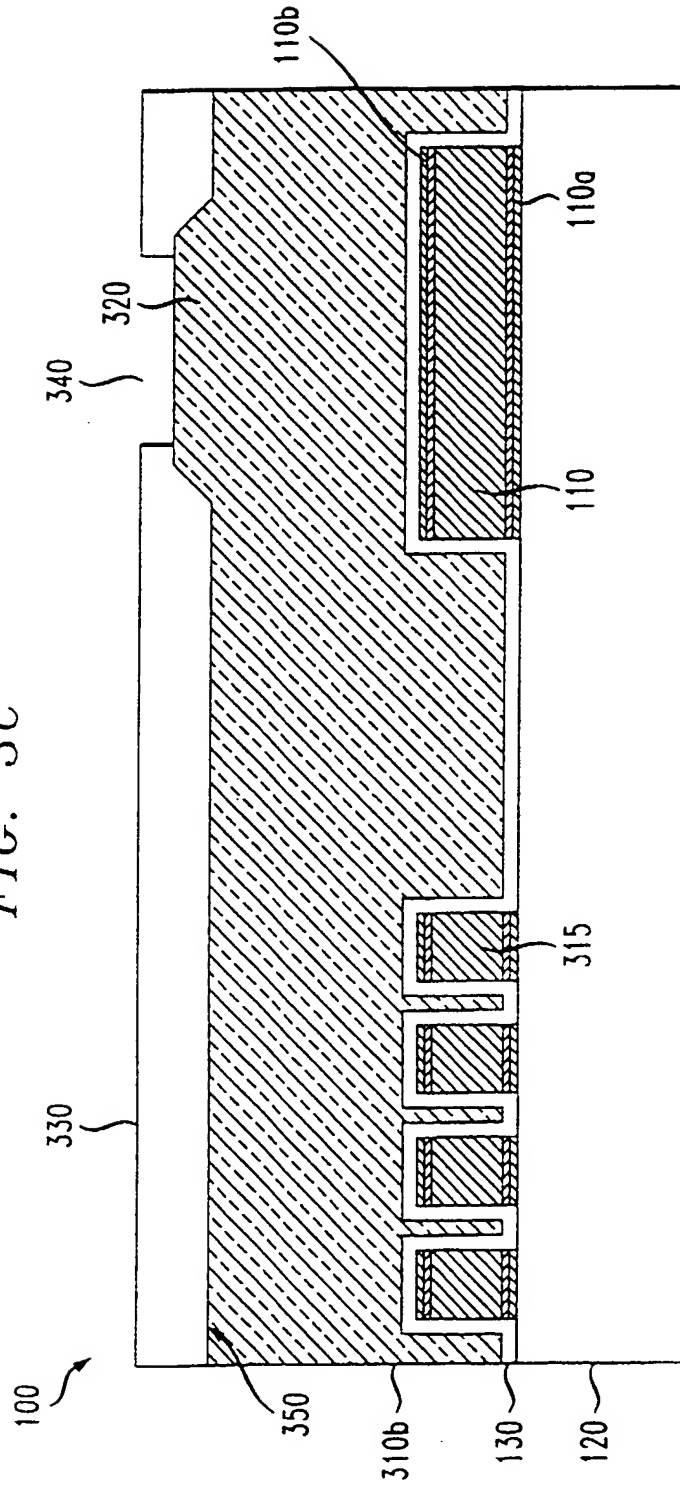
HIGH DENSITY PLASMA-FLUORINATED SILICON
GLASS PROCESS STACK AND METHOD OF MANUFACTURE THEREFOR

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to a semiconductor device and, more
5 specifically, to a semiconductor device having a silicon-rich barrier layer located over a
metal feature on a semiconductor substrate.

BACKGROUND OF THE INVENTION

Current semiconductor technology, as is commonly known, is constantly
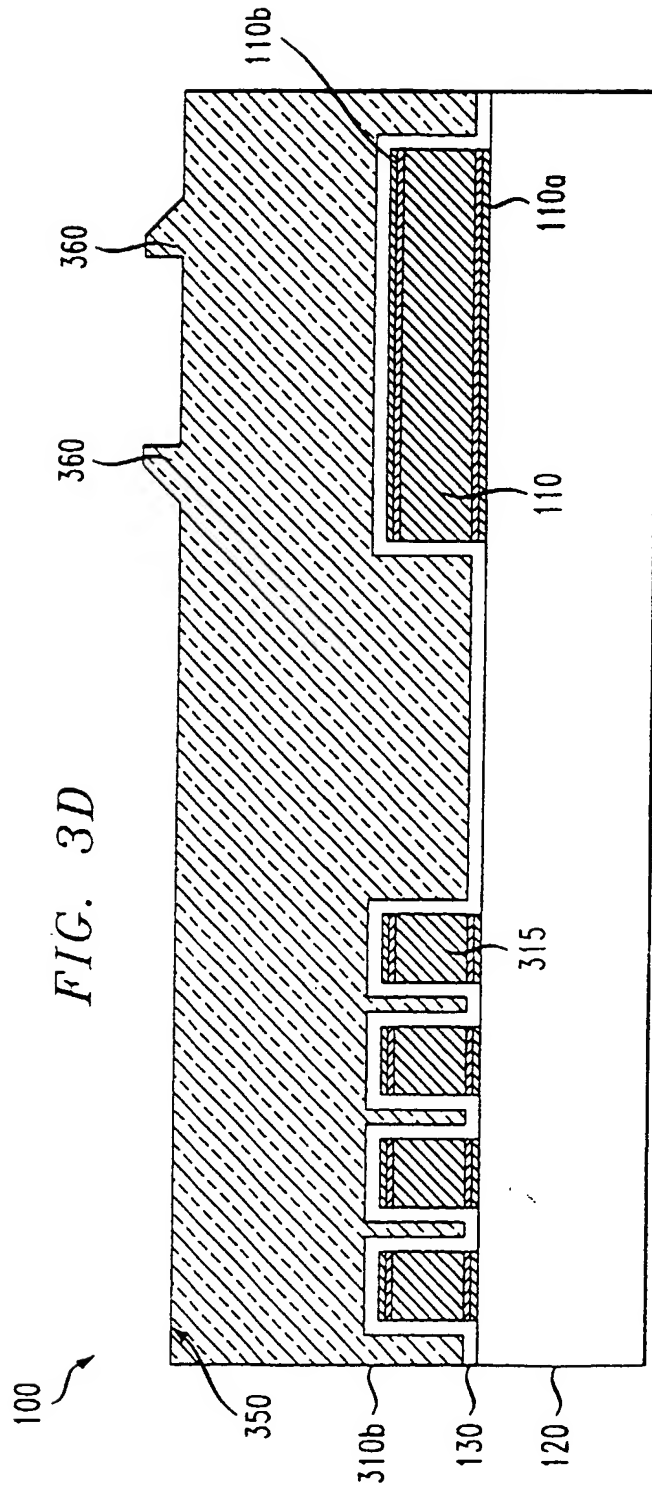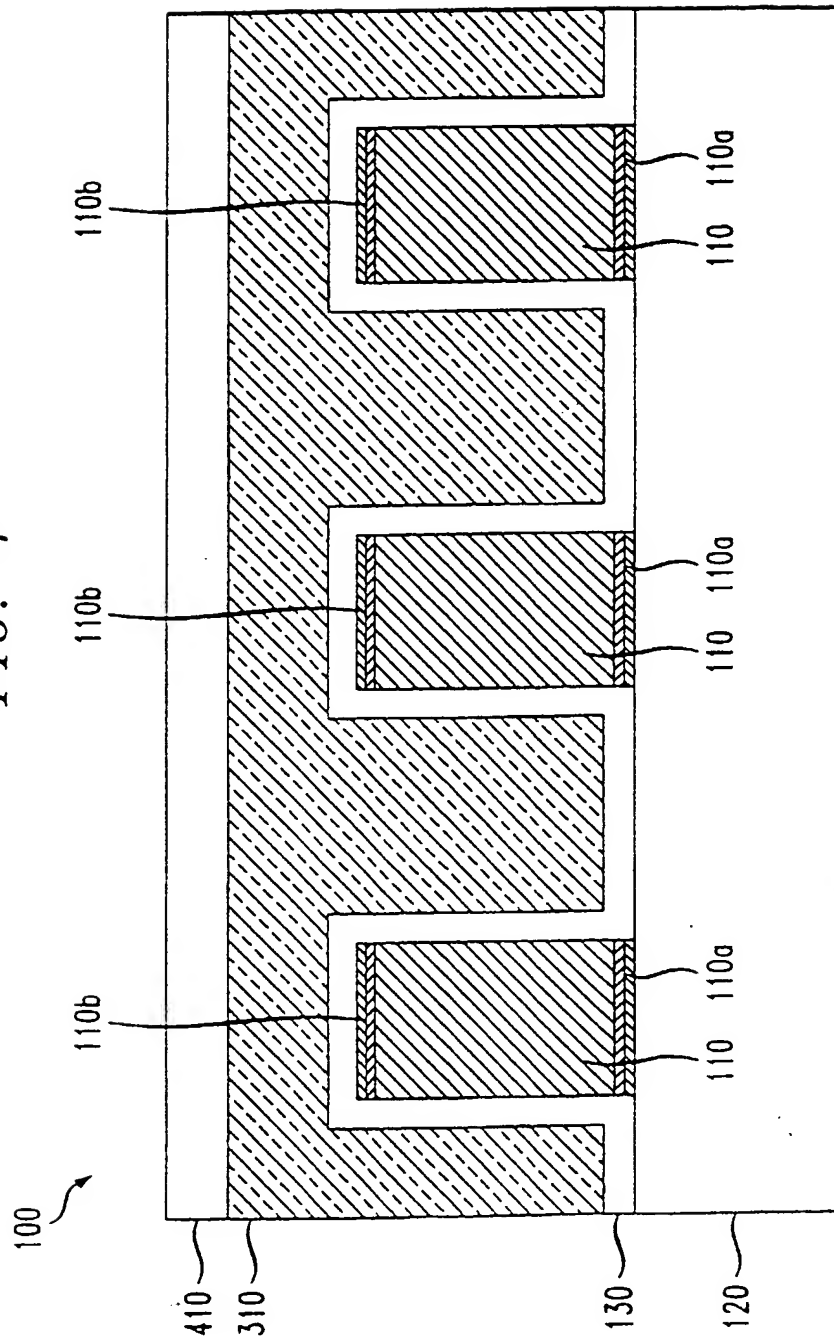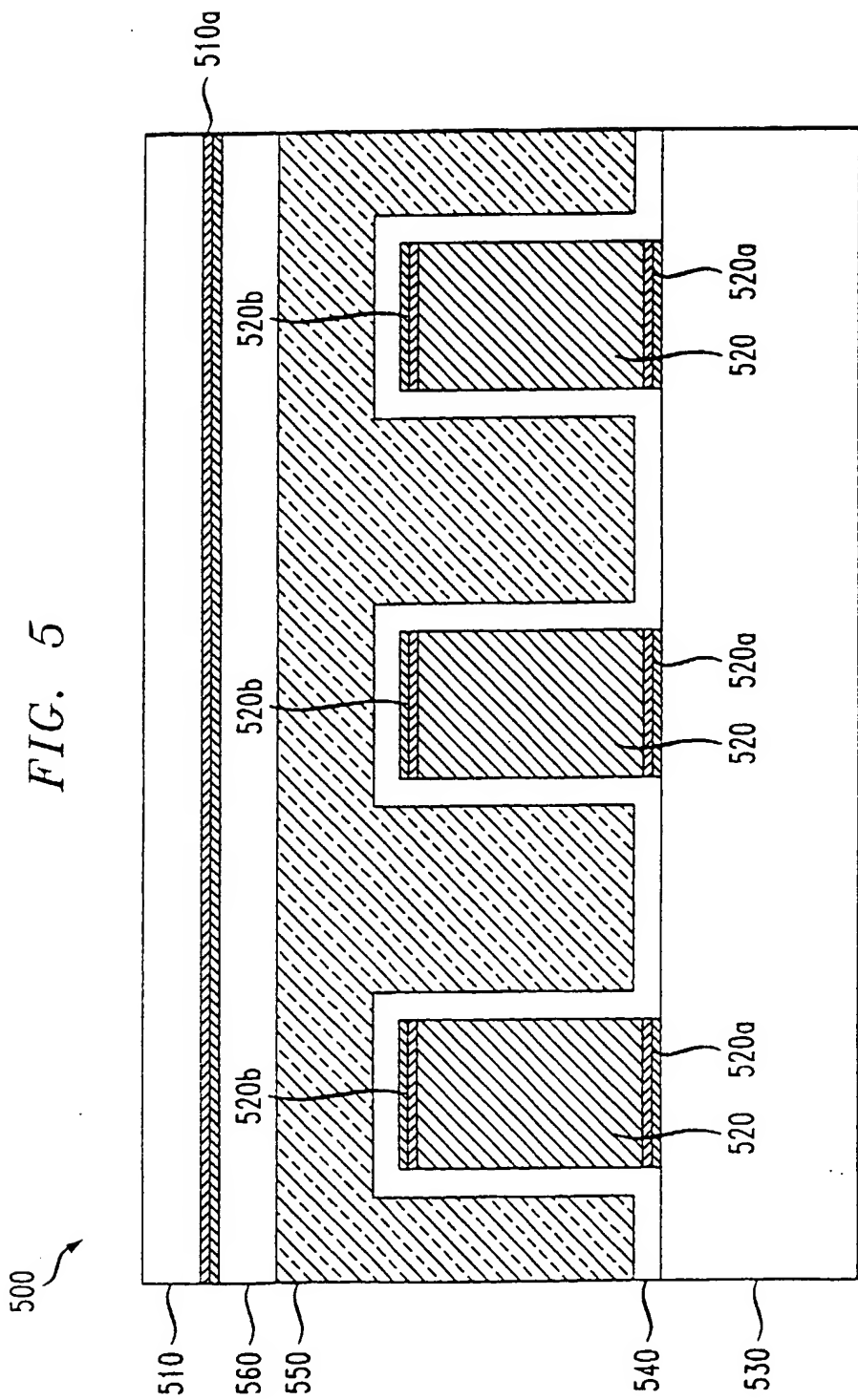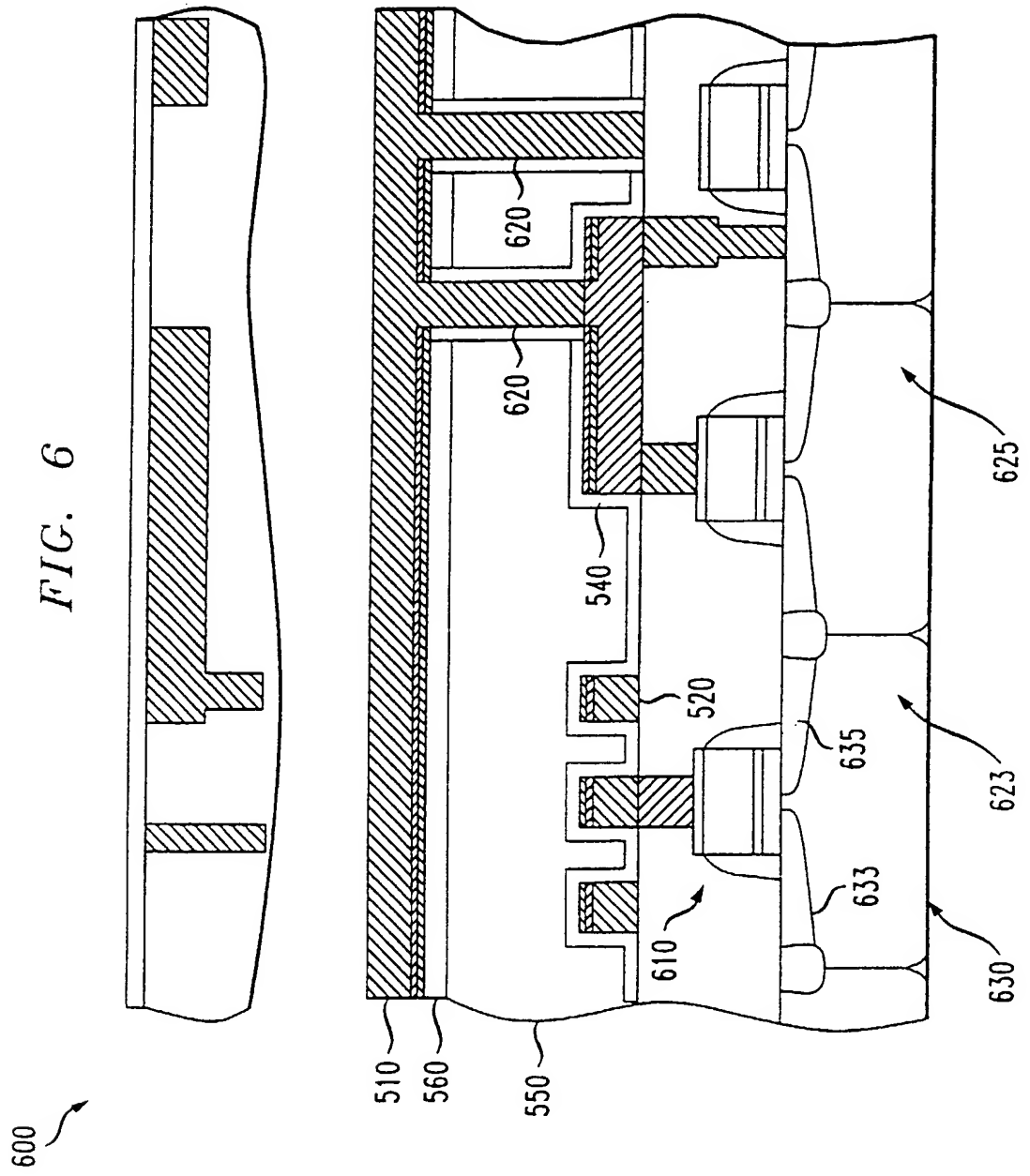decreasing the size of its components. Included in this decrease in size, is the decrease in
10 distance between metal interconnects, either on different metal levels or on a given metal
level. As a result of the overall decrease in device size and the present interlevel dielectric
materials used, RC delays have become a problem. It is believed that the RC delay
problems are a result of the unintentional capacitance coupling that arises between the
metal interconnects and the interlevel dielectric material used.

15 Thus, the semiconductor manufacturing industry in trying to prevent the RC delay
problems associated with the decrease in device size, is currently moving toward using a
low dielectric constant material, such as fluorinated silicon glass (FSG), for the interlevel
dielectrics. The FSG interlevel dielectric material tends to lower the capacitive coupling
between the runners, which then lowers the RC delay in the circuits, providing a faster
20 integrated circuit. However, when integrating FSG into conventional integrated circuits, a
number of difficulties are encountered.

One difficulty is the instability of the fluorine within the FSG dielectric material.
Some of the fluorine is bonded in the FSG dielectric material, while much of the fluorine is
loosely bonded, or not bonded at all. Unfortunately, the loosely bonded and unbonded
25 fluorine tend to move when the integrated circuit encounters large temperature variations.
Such large temperature variations generally occur during the manufacturing process, but
may also arise while using the integrated circuit. Moreover, the movement of the fluorine
within the integrated circuit tends to cause two general problems.

One such problem arises when the unbonded fluorine attacks the metal stack, commonly comprising titanium, located over the FSG interlevel dielectric material. When the metal stack comprises titanium, the fluorine combines with the titanium to form titanium fluoride, which has very poor adhesion properties. Because of the poor adhesion properties, the titanium metal stack tends to buckle and peel away from the FSG dielectric material, causing more problems. Theoretically, metal stacks comprising different materials would also experience similar problems as associated with the titanium metal stacks.

Another problem arising from the movement of the fluorine within the FSG dielectric material occurs when the fluorine combines with a metal feature. Aluminum interconnect lines are commonly used as metal features within semiconductor devices. The fluorine attempts to combine with the aluminum to form aluminum fluoride, which negatively impacts the conductive nature of the aluminum interconnect lines. It is suspected that when fluorine combines with other metals within a conventional integrated circuit, the same result will occur.

Another problem currently encountered in today's semiconductor technology is the inability to inexpensively and accurately planarize a surface of material. While accurate planarization has always been important within the semiconductor manufacturing industry, it has become even more important with the extremely small submicron device sizes associated with present day technologies. As is well known, it is important to achieve effective planarization to conduct a subsequent, accurate, photolithographic process for such submicron feature sizes.

As mentioned above current semiconductor technology deposits a layer of material, typically a dielectric material such as FSG, over features on a semiconductor wafer. Typically, the FSG is deposited using a high density plasma process, which has an isotropic etching component associated with it. The effects of this isotropic component are quite evident across wide features, such as capacitors, inductors, etc., which are frequently incorporated into today's integrated circuit designs. The other features, such as gate structures and interconnect lines, are small enough that the isotropic component leaves

only a small protrusion that is easily and effectively planarized with conventional chemical/mechanical planarization (CMP) processes. However, the wide features present an entirely different problem.

Because the wide feature is higher than the surface that it is located upon, a raised

5 area or anomaly of the deposited material is typically generated above such features due to the isotropic etching effect during deposition. The problem arises when the surface of the semiconductor device, including the raised area, is planarized, typically using a CMP process. Generally, regions containing mainly high areas polish slower than regions containing mostly low areas. This polishing rate differential tends to produce non-

10 uniformity in the material thickness across the chip, which can subsequently affect accuracy, device performance and device yield. Moreover, differences in pattern density between different types of integrated circuits can lead to varying polishing rates, which make manufacturing more difficult and costly.

The semiconductor manufacturing industry, in the past, developed several methods

15 to attempt to minimize pattern density effects during CMP. One method was to alter the various CMP process variables such as down force, carrier speed and polishing pad hardness. Altering the various CMP process variables tended to help; unfortunately, there is a trade-off between die and across wafer uniformity when these variables are changed. Moreover, the differing variables do not influence the polishing rate. Another method

20 attempted was to deposit "dummy" metal features to even out the pattern density. However, its effectiveness depends on the specifics of the circuit layout and the deposition profile of the dielectric material used. Moreover, the "dummy" technique tends to be time consuming and costly.

Accordingly, what is needed in the art is a semiconductor device using an interlevel

25 dielectric comprising a low dielectric constant material such as fluorinated silicon glass (FSG), that does not experience the problems associated with the movement of the unbonded fluorine during large temperature variations. Also needed in the art, is a planarization process that does not experience the polishing rate differential and other polishing problems as associated with the prior art polishing techniques.

SUMMARY OF THE INVENTION

To address the above-discussed deficiencies of the prior art, the present invention provides a semiconductor device that includes a metal feature and a method of manufacture therefor. In an advantageous embodiment, the semiconductor device includes a dielectric layer deposited over a metal features. The dielectric layer includes a material that is capable of diffusing into the metal features. To prevent this diffusion, the semiconductor device includes a silicon-rich barrier layer located on the metal feature that isolates the metal feature from the dielectric layer. The barrier layer inhibits the diffusion of the material of the dielectric layer into the metal feature. Another embodiment introduces a capping layer located over the dielectric layer and a metal feature located over the capping layer. In one exemplary embodiment, the barrier layer, dielectric layer and the capping layer are deposited in-situ in a single deposition chamber.

Thus, in one aspect, the invention provides a semiconductor device that has a barrier layer located over a metal feature of the semiconductor device. The barrier layer makes feasible the use of a low dielectric constant (K) material, such as a fluorinated dielectric material, to reduce the RC delay associated with the integrated circuit.

In another aspect of the invention, the barrier layer is a silicon-rich oxide and the dielectric layer is a dielectric layer having a low dielectric constant, such as fluorinated silicon glass (FSG). The barrier layer and dielectric layer may be formed in the presence of argon, oxygen, and silane gases.

The capping layer may comprise a similar material as the barrier layer and inhibits diffusion of the dielectric layer into the metal feature above the capping layer. The capping layer, in an advantageous embodiment, comprises a silicon-rich oxide. Moreover, the capping layer may, in an alternative embodiment, be formed in the presence of argon, oxygen, and silane gas.

The metal feature, in another aspect, is a metal line comprising aluminum. Moreover, in an alternative aspect, multiple metal features may be located on the semiconductor substrate, and the barrier layer may isolate each of the multiple metal features from the dielectric layer. However, one having skill in the art knows that the

metal line may comprise other similar materials.

The present invention, in an alternative embodiment, includes an integrated circuit. The integrated circuit may include, in another embodiment, transistors and metal features acting as interconnects and electrically connecting the transistors to form the integrated circuit.

Also covered by the present invention is a method of planarizing an interlevel layer located over a feature located on a substrate. In one embodiment, the method includes depositing a dielectric layer over a feature wherein the method for depositing has an isotropic etch component that causes an anomaly not to form over anything but a wide feature. The dielectric layer, in another embodiment, may be a fluorinated silicate glass deposited using a high density plasma process. The method further includes patterning a photoresist to expose a substantial portion of the anomaly, etching the exposed portion to leave remnants of the anomaly, and planarizing, typically using a traditional CMP process, to leave a substantially planar surface.

In another exemplary embodiment, there is presented a semiconductor device that has a metal feature located on a substrate of a semiconductor device. The semiconductor device comprises (1) a dielectric layer, which may include fluorine, that is capable of diffusing into a metal feature that it is located over, (2) a silicon-rich barrier layer located between the metal feature and the dielectric layer, (3) a capping layer located over the dielectric layer, and (4) a metal layer located over the capping layer, wherein the capping layer inhibits a diffusion of the fluorine into the metal layer. Moreover, in another aspect, the barrier layer, dielectric layer and capping layer may be formed by high density plasma in situ.

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the

same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

5   For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a cross-sectional view of a semiconductor device at an intermediate stage of manufacture, including a barrier layer formed over a semiconductor

10   substrate;

FIGURE 2 illustrates a schematic of a low pressure inductively coupled HDP chemical vapor deposition (CVD) reactor;

FIGURE 3A illustrates the semiconductor device illustrated in FIGURE 1, after a deposition of a substantially flat dielectric layer over the metal features and the barrier

15   layer;

FIGURE 3B illustrates the semiconductor device illustrated in FIGURE 1, after a deposition of a dielectric layer having an anomaly over metal feature;

FIGURE 3C illustrates the semiconductor device illustrated in FIGURE 3B after a photoresist material has been deposited and patterned thereon;

20   FIGURE 3D illustrates the semiconductor device illustrated in FIGURE 3C after removal of between about 75% and about 99% of the anomalies, leaving horn like remnants;

FIGURE 4 illustrates the semiconductor device illustrated in FIGUREs 3A-3D after a deposition of a capping layer over the dielectric layer;

25   FIGURE 5 illustrates a completed semiconductor device, after a conventional deposition of a second metal feature; and

FIGURE 6 illustrates a sectional view of a conventional integrated circuit, which might be manufactured according to the principles of the present invention.

DETAILED DESCRIPTION

Referring initially to FIGURE 1, illustrated is a cross-sectional view of a semiconductor device 100 at an intermediate stage of manufacture. Also illustrated in FIGURE 1 are metal features 110 located on a semiconductor substrate 120. The metal features 110 may comprise aluminum that are metal lines that connect different active devices in the semiconductor device 100. Generally, these metal features 110 may also include conventionally formed titanium/titanium nitride (Ti/TiN) layers 110a, 110b. It should be noted that the semiconductor wafer substrate 120 may be any substrate located in a semiconductor device 100, including the wafer itself or a substrate located above the wafer. It should also be noted that the semiconductor device 100 is not limited to three metal features 110 and that a single metal feature 110 or additional multitude of metal features 110 may make up the semiconductor device 100.

Formed over the metal features 110 is a barrier layer 130, which in an advantageous embodiment comprises a silicon-rich oxide. The barrier layer 130 may be deposited using a conventional inductively coupled high density plasma (HDP) process. Turning briefly to FIGURE 2, illustrated is a schematic of a conventional low pressure inductively coupled HDP chemical vapor deposition (CVD) reactor 200. The HDP CVD reactor 200 typically includes a chamber 210, inductive coils 220, a top radio frequency (RF) power source 230, a side RF power source 240 and a bottom RF power source 250.

Turning back to FIGURE 1, with continued reference to FIGURE 2, to form the barrier layer 130 the semiconductor device 100 is typically placed within the chamber 210 of the HDP CVD reactor 200. Next, about 1500 watts of power is applied to the top power source 230 and about 2500 watts of power is applied to the side power source 240, while flowing a mixture of argon, oxygen and silicon gas over the surface of the semiconductor device 100. Furthermore, a limited amount of power may be applied to the bottom power source 250 to aid in filling the gaps between the metal features 110, after the HDP process has already begun. However, if the bottom power source is applied too early, it can chisel away at the corners of the metal features 110, possibly causing a short. The gas commonly used to form the barrier layer 130 is silane (SiH_4), however other gases may be used. What

results is the barrier layer 130, preferably having a thickness of about 50 nm and a refractive index of about 1.51. One having skill in the art knows that other deposition processes could be used, the deposition parameters could be altered, and the thickness could be changed, as long as each of the changes is consistent with the design of the

5   device.

Turning to FIGURE 3A with continued reference to FIGURE 2, shown is the semiconductor device 100 illustrated in FIGURE 1, after a deposition of a substantially planar dielectric layer 310a over the metal features 110 and the barrier layer 130. The dielectric layer 310a, like the barrier layer 130, is typically deposited using the HDP

10   process. Preferably, the dielectric layer 310a is a low dielectric constant (K) layer such as fluorinated silicon glass (FSG) and is deposited to a thickness of about 600 nm and having a refractive index of about 1.44. Low K typically refers to a material having a dielectric constant less than about 4.0. After the semiconductor device 100 is placed within the HDP CVD reactor chamber 210, about 1200 watts of power is applied to the top power source

15   230, about 3000 watts of power is applied to the side power source 240 and about 2400 watts of power is applied to the bottom power source 250. This is all accomplished while flowing a mixture of argon, oxygen and silane over the surface of the semiconductor device 100. A mixture of gas commonly used to form the dielectric layer 310a is SiH_4 and SiF_4.

20   Ideally, the dielectric layer 310a is deposited using a technique that would provide a substantially planar surface having no anomalies in the dielectric layer 310a located over the features 110. However, HDP processes tend to cause an anomaly 320 in the dielectric layer 310b, as illustrated in FIGURE 3B. Because of an isotropic etch component associated with the HDP process, the anomaly 320 is prevented from forming over a small

25   feature 315. However, the anomalies 320 still form over wide features 110. The anomaly 320 typically has a width less than the wide feature 110 over which it is located. A wide feature is generally a feature having a width that is sufficient to produce a substantial anomaly; that is one that would result in a non-planar surface after CMP and without using the process covered by the present invention. An exemplary width of such a feature may

be a width greater than about 5000 nm. However, smaller widths, which produce anomalies that require the presently described processes to achieve a substantially planar surface, may also fall within the scope of the present invention.

In contrast, the small feature, such as features 315 illustrated in FIGURE 3B, are

5 features that either leave no anomaly after the HDP process or leave only small, sharp features, such as small protrusions or horns. Because such small features 315 typically have a high aspect ratio, they are easily removed by conventional CMP processes without affecting the desired degree of planarity and without the need of further etching. As such, the subsequent patterning and etching process, as provided herein, are impractical or

10 unnecessary to achieve a substantially planar surface. It should be noted that a substantially planar surface is one on which subsequent photolithographic processes can be conducted to accurately form features within design specifications.

Turning to FIGURE 3C, illustrated is a deposition of a photoresist material 330, the photoresist material 330 having been patterned to expose a substantial portion 340 of the

15 anomaly 320. Typically, a mask having an opening having a width less than a width of the anomaly 320 is used to expose the photoresist. An exposed portion 340 is then subjected to a conventional etch. For example a plasma etch, a reactive ion etch or other similar etch could be used to remove the exposed portion 340 of the anomaly 320. The etch, in a preferred embodiment, removes between about 75% and about 99% of the anomaly 320,

20 and etches down to the field level 350 of the dielectric layer 310b.

What results after the etch, are remnants of the anomaly 360 as illustrated in FIGURE 3D. The remnants 360 are preferably horns or protrusions that have a high aspect ratio. In the illustrated embodiment, the remnants have a width that is less than about 1000 nm. The dielectric layer 310b is then planarized. Due to their high aspect ratio the

25 remnants 360 are easily removed, to provide a substantially planar surface, using a traditional chemical mechanical planarization (CMP) process. Thus, the planarization if needed, is accomplished while at least substantially reducing the polishing rate differential and other polishing problems associated with the prior art planarization processes.

After deposition of the dielectric layer 310a or 310b and removal of the anomalies

320 (FIGURE 3B) if needed, a capping layer 410 may be deposited over the dielectric layer 310a, as illustrated in FIGURE 4. In an advantageous embodiments, the capping layer 410 comprises a similar material as found in the barrier layer 130, such as silicon-rich oxide. Analogous to the deposition of the barrier layer 130 and dielectric layer 310a, 310b,

5   the capping layer 410 is generally deposited using the HDP process. Moreover, the capping layer 410 is preferably deposited to a thickness of about 400 nm and having a refractive index of about 1.51. The capping layer 410 is preferably deposited by applying 1500 watts to the top power source 230 and 2500 watts to the side power source 240 while flowing a mixture of argon, oxygen and a silane gas over the semiconductor device 100.

10   The HDP process is not the only deposition process that might be used. For example, other conventional CVD and PVD processes might be used. However, using another non-conformal deposition process might require a standard chemical mechanical planarization (CMP) of the capping layer 410 prior to completing the semiconductor device.

Because the barrier layer 130, the dielectric layer 310 and the capping layer 410

15   may be deposited with high density plasma, all three of these layers may, therefore, be deposited in-situ within the same deposition chamber. In-situ deposition is commonly accomplished by placing the partially completed semiconductor device 100 (FIGURE 1) within the HDP CVD reactor chamber 210 and varying the amount of radio frequency (RF) applied, location where the power is applied, gas mixture, temperature, etc. to arrive

20   at the semiconductor device illustrated in FIGURE 4. Moreover, forming the layers 130, 310, 410, in-situ is particularly advantageous when the underlying features have a width less than about 5000 nm or a width such that the HDP process does not form an anomaly that requires CMP removal, as discussed above. When the width of the feature falls within the parameters just discussed above, the isotropic etching component of the HDP process

25   substantially eliminates the need for an intermediate planarizing steps. An in-situ deposition of the barrier layer 130, dielectric layer 310 and capping layer 410 in a single processing step is highly desirable because it saves money and reduces processing steps. Thus, the single step in situ process could provide additional benefits to the present invention.

Turning to FIGURE 5, illustrated is a completed semiconductor device 500, after a conventional deposition of a second metal feature 510 and Ti/TiN layers 510a. The completed semiconductor device 500 also includes metal features 520 having Ti/TiN layers 520a, 520b located on a semiconductor substrate 530, and a barrier layer 540 located

5   on the metal features 520. Located over the barrier layer 540 is a dielectric layer 550 and a capping layer 560. As illustrated, the barrier layer 540 isolates the metal features 520 from the dielectric layer 550, and inhibits fluorine diffusion from the dielectric layer 550 into at least a portion of the metal features 520. Likewise, the capping layer 560 inhibits diffusion of a material, such as fluorine, of the dielectric layer 550 into the second metal feature 510

10   and Ti/TiN layers 510a, 510b.

Turning briefly to FIGURE 6, there is illustrated a sectional view of a conventional integrated circuit 600, that might be manufactured according to the principles of the present invention. The integrated circuit 600 may include CMOS devices, BiCMOS devices, Bipolar devices, EEPROM devices, including Flash EPROMS, or any other type

15   of similar device. Also shown in FIGURE 6, are components of the conventional integrated circuit 600, including: transistors 610, the metal features 520, the barrier layer 540, the capping layer 560, the second metal feature 510, and the dielectric layer 550. The metal features 520 along with interconnect structures 620 form part of an interconnect system that electrically connects the transistors 610 to form an integrated circuit 600. Also

20   illustrated, are conventionally formed tubs, 623, 625, source regions 633 and drain regions 635, all located over a substrate 630.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

dielectric layer to inhibit a diffusion of a material of the dielectric layer into the metal feature

21.   A method of planarizing an interlevel layer located over a feature located on a semiconductor substrate, comprising:

depositing a dielectric layer over a feature, the depositing having an isotropic etch component that causes an anomaly to form over the feature and in a surface of the dielectric layer;

patterning a photoresist over the dielectric layer to expose a substantial portion of the anomaly;

etching the exposed portion to leave remnants of the anomaly; and

planarizing the dielectric layer to a substantially planar surface.

22.   A method of manufacturing an integrated circuit, comprising:

forming features on a semiconductor substrate;

planarizing interlevel layers having an anomaly, including:

depositing a dielectric layer over the feature, the depositing having an isotropic etch component that causes an anomaly to form over the feature and in a surface of the dielectric layer;

patterning a photoresist to expose a substantial portion of the anomaly;

etching the exposed portion to leave remnants of the anomaly; and

planarizing the interlevel layer to a substantially planar surface; and

forming interconnect structures located within the dielectric layers to interconnect the features to form an operational integrated circuit.

23.   A semiconductor device having a metal feature located on a substrate of the semiconductor device, comprising:

a dielectric layer located over a metal feature and including fluorine that is capable of diffusing into the metal feature; and

a silicon-rich barrier layer located between the metal feature and the dielectric layer;

a capping layer located over the dielectric layer; and

a metal layer located over the capping layer, the capping layer inhibiting a diffusion of the fluorine into the metal layer.

24. A method of forming a semiconductor device including a metal feature located on a semiconductor substrate, comprising:

forming a silicon-rich barrier layer over a metal feature; and

forming a dielectric layer including fluorine over the metal feature and the barrier layer, the silicon-rich barrier layer preventing a diffusion of the fluorine into a metal feature over which the silicon-rich barrier layer is located; and

forming a capping layer over the dielectric layer, wherein the silicon-rich barrier layer, the dielectric layer and the capping layer are formed with a high density plasma in-situ.

The Patent Office

Application No:	GB 0108357.5	Examiner:	Steven Morgan
Claims searched:	1-20, 23 & 24	Date of search:	24 January 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

　　UK Cl (Ed.T): H1K (KJAB,KJAX)

　　Int Cl (Ed.7): H01L 21/768, 23/522, 23/532

Other:　Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2 319 818 A	(NEC) See line 3, page 20 - line 22, page 21.	1-5, 7-14, 16-20, 23 & 24
E,X,&	US 6 277 730 B1	(MATSUSHITA) See whole document.	1-11, 13, 16-20, 23 & 24
X,Y,&	JP 11 317 454 A	(MATSUSHITA) See abstract.	X: 1-11, 13, 16-20, 23 & 24 Y: 12, 14 & 15
Y	EP 0 883 166 A2	(APPLIED MATERIALS) See line 11, column 15 - line 44, column 19.	15
Y	WO 98/28465 A1	(LAM RESEARCH) See for example lines 11-16, page 17.	12 & 14